WHAT IS CLAIMED IS:

1. A method of testing a mask pattern, comprising:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern; and

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other.

2. The method as set forth in claim 1, wherein a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, ···), and first to N-th processes are different from one another.

3. The method as set forth in claim 1, further comprising:

dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

4. The method as set forth in claim 1, wherein said first pattern is a pattern

for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer.

5. The method as set forth in claim 4, wherein said third area is comprised of said contact area and an ambient area surrounding said contact area.

6. The method as set forth in claim 1, wherein said first pattern is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

7. The method as set forth in claim 6, wherein said fourth area is comprised of said fifth area and an ambient area surrounding said fifth area.

8. A program for causing a computer to carry out a method of testing a mask pattern, steps executed by said computer in accordance with said program including:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern; and

(f) checking whether a dimensional gap between said first pattern and said

resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other.

9. The program as set forth in claim 8, wherein a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, ···), and first to N-th processes are different from one another.

10. The program as set forth in claim 8, wherein said steps further include:

dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

11. The program as set forth in claim 8, wherein said first pattern is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer.

12. The program as set forth in claim 11, wherein said third area is comprised of said contact area and an ambient area surrounding said contact area.

13. The program as set forth in claim 8, wherein said first pattern is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting

said active area onto said first pattern.

14. The program as set forth in claim 13, wherein said fourth area is comprised of said fifth area and an ambient area surrounding said fifth area.

15. A method of forming a mask having a desired mask pattern, including:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern;

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs; and

(g) transferring said mask pattern onto a mask,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other.

16. The method as set forth in claim 15, wherein a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, ···), and first to N-th processes are different from one another.

17. The method as set forth in claim 15, further comprising:

dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

18. The method as set forth in claim 15, wherein said first pattern is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer.

19. The method as set forth in claim 18, wherein said third area is comprised of said contact area and an ambient area surrounding said contact area.

20. The method as set forth in claim 15, wherein said first pattern is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.